CS221: Logic Design



## Assignment no 8: Chapter 9

Note: You can check the exercises after the book Chapter. In our assignment, we are using the 11<sup>th</sup> edition of "Digital Fundamentals" By Thomas L. Floyd"

**4.** For the ripple counter in Figure 9–66, show the complete timing diagram for sixteen clock pulses. **Show** the clock,  $Q_0$ ,  $Q_1$  and  $Q_2$  waveforms.



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FIGURE 9-66
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8. Show the complete timing diagram for the 5 stage synchronous binary counter in Figure 9–67, verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.





## CS221: Logic Design

**10.** The waveforms in Figure 9–69 are applied to the count enable, clear, and clock inputs as indicated. **Show** the counter output waveforms in proper relation to these inputs. The clear input is asynchronous.



FIGURE 9-69

FIGURE 9-73

**12.** The waveforms in Figure 9–71 are applied to a 74HC163 binary counter. **Determine** the Q outputs and the RCO. The inputs are  $D_0 = 1$ ,  $D_1 = 1$ ,  $D_2 = 0$ , and  $D_3 = 1$ .



**18. Determine** the sequence of the counter in Figure 9–73.



## **CS221: Logic Design**



**20. Design** a counter to produce the following sequence. Use J-K flip-flops.

00, 10, 01, 11, 00, ...

22. Design a counter to produce the following binary sequence. Use J-K flip-flops.

0, 9, 1, 8, 2, 7, 3, 6, 4, 5, 0, ...

23. Design a binary counter with the sequence shown in the state diagram of Figure 9–7°.



FIGURE 9-75